IN THE CLAIMS

Please amend the claims as shown below. Claim 2 is amended below. Please cancel Claims 11-23 without prejudice. This listing of claims replaces all prior versions and listings of claims in the Application.

1. (Original) For an electronic architecture with a functional constitution, said functional constitution performing a number of architectural functions characterized by separate stages, a method of deriving a benchmark program for maximum power consumption prior to an implementation of said architecture, said method comprising:

modeling a functional model of said architecture;

compiling said benchmark program into a corresponding instruction stream;

valuating a power weight for each said stage of each said function of each said constituent;

running said model in a maximum power consumption mode; and

summarizing said power consumption.

2. (Currently Amended) The method as recited in Claim 1, wherein said functional model comprises a representation of said functional constitution of said architecture at a high level of abstraction capable of simulating the functioning of said architecture and said functional constitution thereof, the total power consumption of said architecture and of said functional constitution thereof,

wherein said benchmark delineates power consumption of said architecture and said functional constitution thereof [[is]] in terms of maximum power.

3. (Original) The method as recited in Claim 2, wherein said modeling a functional model of said architecture further comprises writing a program in SystemC.

4. (Original) The method as recited in Claim 1, wherein said compiling said benchmark program into a corresponding instruction stream is performed by a compiler.

5. (Original) The method as recited in Claim 4, wherein said compiler is a PERL script.

6. (Original) The method as recited in Claim 1, wherein said valuating a power weight for each said stage of each said function of each said constituent further comprises:

selecting each of said architectural functions individually;

determining the characteristic technology of each of said architectural functions selected;

counting a number of technology gates constituting each of said architectural functions selected;

determining a power weight for each of said technology gates; and

deriving a power weight for each of said architectural functions selected.

7. (Original) The method as recited in Claim 6, wherein said selecting each of said architectural functions individually further comprises:

determining if said architectural functions selected are memory type functions;

itemizing individual memory subfunctions; and

treating each of said individual memory subfunctions as separate, equivalent, distinct architectural functions.

8. (Original) The method as recited in Claim 6 wherein said deriving a power weight for each of said architectural functions selected comprises multiplying said power weight determined for each of said technology gates by said number of said technology gates.

9. (Original) The method as recited in Claim 1, wherein said running said model in a maximum power consumption mode comprises running a power virus program.

10. (Original) The method as recited in Claim 1, wherein said architecture is a microprocessor.

11-23. (Cancelled)